

In the Specification:

Please insert the following subtitle and three paragraphs after the title on page 1:

--CROSS-REFERENCE TO RELATED APPLICATIONS--

Ack B1
--This application is a division of Serial No. 09/426,056, filed October 22, 1999. *AA*

LAK 1/23/02
A
--The subject matter of this application relates to the subject matter of copending Catabay, Hsia,
Li, and Zhao U.S. Patent Application Serial No. 6,391,795
entitled "LOW DIELECTRIC
CONSTANT SILICON OXIDE-BASED DIELECTRIC LAYER FOR INTEGRATED CIRCUIT
STRUCTURES HAVING IMPROVED COMPATIBILITY WITH VIA FILLER MATERIALS,
AND METHOD OF MAKING SAME", filed by one of us with others on October 22, 1999,
assigned to the assignee of this application, and the subject matter of which is hereby
incorporated herein by reference. *A*

Ack B2
1/23/02
--The subject matter of this application relates to the subject matter of copending Li, Catabay,
and Hsia U.S. Patent Application Serial No. 6,423,628
entitled "INTEGRATED CIRCUIT
STRUCTURE HAVING LOW DIELECTRIC CONSTANT MATERIAL AND HAVING
SILICON OXYNITRIDE CAPS OVER CLOSELY SPACED APART METAL LINES", filed
by one of us with others on October 22, 1999, assigned to the assignee of this application, and
the subject matter of which is hereby incorporated herein by reference. *A*

Please replace the paragraph beginning at page 3, line 16, with the following rewritten paragraph:

--In one embodiment in the aforementioned Serial No. 09/426,061, low k silicon oxide dielectric material having a high carbon doping level is formed in the high aspect regions between closely spaced apart metal lines and then a second layer comprising a low k silicon oxide dielectric material having a lower carbon content is then deposited over the first layer and the metal lines.

However, since both layers are formed by the Trikon process, the deposition rate does not radically change.⁴

Please replace the paragraph beginning at page 3, line 27, with the following rewritten paragraph:

LAC sub *1/23/02* *PATENT* *6,423,628*
In the aforementioned Serial No. 09/425,552, a layer of silicon oxynitride (SiON) is formed over the top surface of the metal lines to serve as an anti-reflective coating (ARC), a hard mask for the formation of the metal lines, and a buffer layer for chemical mechanical polishing (CMP). Low k silicon oxide dielectric material having a high carbon doping level is then formed in the high aspect regions between closely spaced apart metal lines up to the level of the silicon oxynitride. CMP is then applied to planarize the upper surface of the low k carbon-doped silicon oxide dielectric layer, using the SiON layer as an etch stop, i.e., to bring the level of the void-free low k silicon oxide dielectric layer even with the top of the SiON layer. A conventional (non-low k) layer of silicon oxide dielectric material is then deposited by plasma enhanced chemical vapor deposition (PECVD) over the low k layer and the SiON layer. A via is then cut through the second dielectric layer and the SiON to the top of the metal line. Since the via never contacts the low k layer between the metal lines, via poisoning due to exposure of the low k layer by the via does not occur.

Please replace the paragraph beginning at page 8, line 7, with the following rewritten
paragraph:

--Such void-free low k silicon oxide dielectric material may be deposited by reacting hydrogen peroxide with a carbon-substituted silane such as methyl silane, as described in Dobson U.S. Patent No. 5,874,367, the subject matter of which is hereby incorporated by reference. The void-free low k silicon oxide dielectric material may also be deposited by reacting a mild oxidant such as hydrogen peroxide with the carbon-substituted silane materials disclosed in Aronowitz et al. U.S. Patent 6,303,047, and assigned to the assignee of this application, the subject matter of which is also hereby incorporated by reference. *JK*